ACE25QC800GD

8M Bit SERIAL FLASH MEMORY

Description

ACE25QC800GD is 8Mb bits Serial NOR Flash, the array is organized into 4096 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 4 (1Kb sector erase), groups of 16 (4KB Sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase), The device operates on a single 1.65V to 3.6V power supply with current consumption as low as 1mA active and 0.1μA for power-down. All devices are offered in space-saving packages.

The ACE25QC800GD supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 120MHz are supported allowing equivalent clock rates of 240MHz (120MHz x 2) for Dual I/O and 480MHz (120MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. A Hold pin, Write Protect pin and programmable write protection, with top, bottom or complement array control, provide further control flexibility.

Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique ID. ACE25QC800GD features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (CLK), a serial data input (DI), and a serial data output (DO). Serial access to the device is enabled by CS# input.

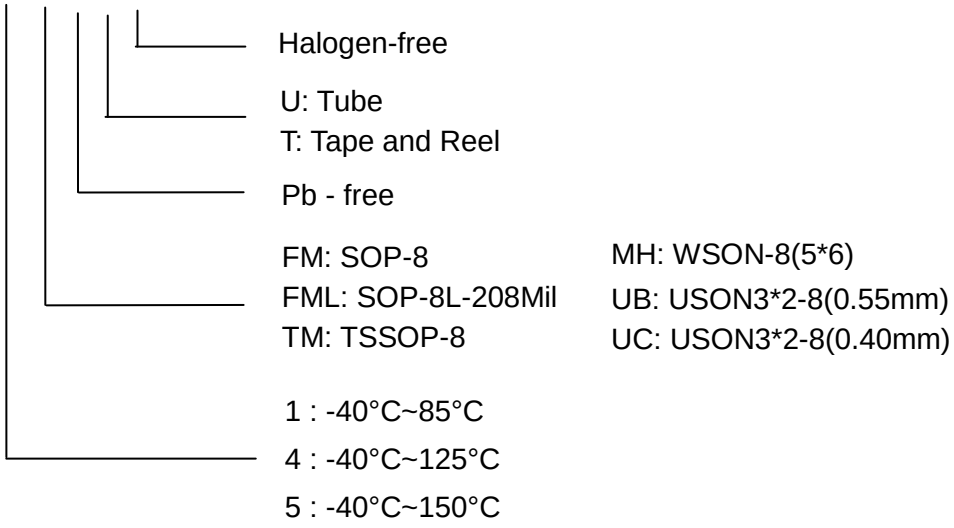
Features

- 8M/bit Serial Flash
  - 1M-byte
  - 256 bytes per programmable page
- Single Power Supply Voltage: Full voltage range: 1.65~3.6V
- Standard, Dual, Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: CLK, CS#, IO0, IO1, IO2, IO3
- High Speed Clock Frequency
  - 80MHz (1.65~2.3V),120MHz (2.3~3.6V)
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
  - Quad I/O Data transfer up to 480Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection

- Allows XIP (execute in place) Operation
  Continuous Read With 8/16/32/64-byte Wrap
- Fast Program/Erase Speed
  Page Program time:1.25ms typical
  Sector Erase time: 2.5ms typical
  Block Erase time: 2.5ms typical
  Chip Erase time: 5ms typical
- Flexible Architecture
  Uniform Sector of 1K-byte
  Uniform Sector of 4K-byte
  Uniform Block of 32/64K-byte
  Erase/Program Suspend/Resume
- Low Power Consumption
  7uA typical Standby current
  0.1uA typical power down current
- Advanced security Features
  4*256-Byte Security Registers With OTP Lock
  64-Bit Unique Serial Number for each device
- Minimum 200,000 Program/Erase Cycles
- ESD protection (Human Body Model): -6500V to 6500V
- Data Retention: 50-year data retention typical

Ordering Information

ACE25QC800GD X XX + X H



Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Technology Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.